

(19) World Intellectual Property  
Organization  
International Bureau



529982

(43) International Publication Date  
3 June 2004 (03.06.2004)

PCT

(10) International Publication Number  
**WO 2004/046750 A2**

(51) International Patent Classification<sup>7</sup>:

G01S

(74) Agent: LONG, Daniel, J.; Bae Systems Information and Electronic Systems Integration Inc., 65 Spit Brook Road, NHQ01-719, Nashua, NH 03061 (US).

(21) International Application Number:

PCT/US2003/037042

(22) International Filing Date:

17 November 2003 (17.11.2003)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

60/427,494 19 November 2002 (19.11.2002) US

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(71) Applicant (*for all designated States except US*): BAE SYSTEMS INFORMATION AND ELECTRONIC SYSTEMS INTEGRATION, INC. [US/US]; 65 Spit Brook Road, NHQ01-719, Nashua, NH 03061 (US).

(72) Inventor; and

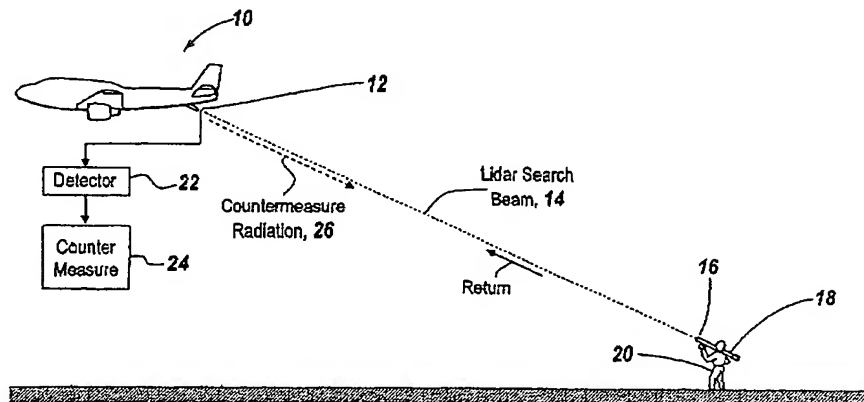
(75) Inventor/Applicant (*for US only*): WEBER, Jonathan, L. [US/US]; 8 Scott Avenue, Nashua, NH 03062 (US).

Published:

— without international search report and to be republished upon receipt of that report

[Continued on next page]

(54) Title: IMPROVED ACTIVE SENSOR RECEIVER DETECTOR ARRAY FOR COUNTERMEASURING SHOULDER-FIRED MISSILES



(57) Abstract: A focal plane architecture is provided which includes direct reading of an array of infrared detectors, each coupled to its own threshold circuit, the output of which is coupled to one input of a NAND gate, with the other input to the NAND gate being provided with a delayed threshold circuit output, thus to permit discrimination against ground clutter. This architecture results in an ultra fast frame read out, inherent discrimination of compact targets, photon counting at infrared wavelengths, and programmable range gating by exterior selection of array events within an expected return time for a transmitted pulse.

WO 2004/046750 A2